GAMMA VOLTAGE GENERATOR AND METHOD THEREOF FOR GENERATING INDIVIDUALLY TUNABLE GAMMA VOLTAGES

FIELD OF THE INVENTION

The present invention relates generally to a gamma voltage generator and gamma voltage generating method, and more particularly, to a gamma voltage generator and method thereof to generate a plurality of gamma voltages that can be individually adjusted.

BACKGROUND OF THE INVENTION

Thin film transistor liquid crystal display (TFT-LCD) requires gamma voltage generator to generate gamma voltages corresponding to a gamma curve related to the characteristics of the TFT-LCD to adjust its display effect. Specifically, the gamma curve is typically symmetric in the manner that it has a central gamma voltage and two groups of gamma voltages symmetric to each other with the central gamma voltage as the symmetric center thereof. Fig.

1 shows a conventional gamma voltage generator 10, which comprises a voltage divider 12 connected between a supply voltage V_S and ground GND, and the voltage divider 12 is composed of several resistors R_1, R_2, R_3, ..., R_{k+1} connected in series, so as to divide the supply voltage V_S to be several voltages V_{R1}, V_{R2}, V_{R3}, ..., V_{Rk} that are further buffered by respective operational amplifiers AMP_1, AMP_2, AMP_3, ..., AMP_k to output the gamma voltages V_{G1}, V_{G2}, V_{G3}, ..., V_{Gk}. Since the gamma voltage generator 10 generates the gamma voltages by the voltage divider 12 composed of several resistors connected in series, whenever any one among these resistors in the voltage divider 12 is adjusted to tune the corresponding gamma voltage, all the other gamma voltages are also altered in the same time. In order to keep the other gamma voltages correct, any tuning among these gamma voltages requires the overall change of the resistors, and which is time-consuming and inconvenient in use.

To improve the above disadvantage, another gamma voltage generator 20 is proposed, as shown in Fig. 2, in which the gamma voltages V_{G1}, V_{G2}, V_{G3}, ..., V_{Gk} are generated from a supply voltage V_S divided by resistor pairs [R_{10}, R_{12}], [R_{20}, R_{22}], [R_{30}, R_{32}], ..., [R_{k0}, R_{k2}], respectively. When the gamma voltage generator 20 is desired to be adjusted with any one of the gamma voltages V_{G1}, V_{G2}, V_{G3}, ..., V_{Gk}, only the corresponding resistor pair is changed. Even though the gamma voltage generator 20 can be adjusted with its

gamma voltages individually, the number of the resistors that are external to the chip they are connected is twice of that required by the gamma voltage generator 10, and as a result, the circuit of the gamma voltage generator 20 becomes more complex. Moreover, the chip using such gamma voltage generators is required to prepare more pins for the generated gamma voltages.

Therefore, it is desired a gamma voltage generator that requires less pins when it is used and is able to individually tune the gamma voltages it generates.

SUMMARY OF THE INVENTION

An object of the present invention is to propose a gamma voltage generator and gamma voltage generating method that is able to tune the gamma voltages individually.

Another object of the present invention is to propose a gamma voltage generator and gamma voltage generating method that requires fewer pins for the chip to connect thereto.

In a gamma voltage generator and gamma voltage generating method, according to the present invention, a plurality of variable resistive elements are supplied respectively with a plurality

of gamma currents of a same magnitude from a current source to generate a variable common voltage and a plurality of variable voltages, from which a common gamma voltage and a plurality of first gamma voltages are generated, a mirror mapping circuit generates a plurality of mapped voltages from the first gamma voltage with the common gamma voltage as a reference and from which a plurality of second gamma voltages are generated. The first and second gamma voltages are symmetric to each other with the common gamma voltage as the central axis, and the common gamma voltage and the first and second gamma voltages are thus provided for the gamma voltages corresponding to a gamma curve.

BRIEF DESCRIPTION OF DRAWINGS

These and other objects, features and advantages of the present invention will become apparent to those skilled in the art upon consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows a conventional gamma voltage generator;

Fig. 2 shows another conventional gamma voltage generator;

Fig. 3 shows a gamma voltage generator according to the present invention;

Fig. 4 shows a current mirror for the gamma voltage generator shown in Fig. 3;

Fig. 5 shows a gamma curve of the gamma voltage generator shown in Fig. 3;

Fig. 6 shows an embodiment mirror mapping circuit for the gamma voltage generator shown in Fig. 3; and

Fig. 7 shows another embodiment mirror mapping circuit for the gamma voltage generator shown in Fig. 3.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 3 shows a gamma voltage generator 100 according to the present invention, which comprises several independent voltage sources 102 to 112 to provide a variable common voltage V_{COM} and several variable voltages V_1 to V_5 to buffer operational amplifiers 114 to 124, to further generate a common gamma voltage V_{GCOM} and several gamma voltages V_{G1} to V_{G5}, and a mirror mapping circuit 136

to generate several mapped voltages V_6 to V_{10} by mapping the gamma voltages V_{G1} to V_{G5} with the common gamma voltage V_{GCOM} as a reference to buffer operational amplifiers 126 to 134 to further generate gamma voltages V_{G6} to V_{G10}. In the voltage sources 102 to 112, several variable resistors R_{COM} and R_1 to R_5 each is supplied with a gamma current I_S that has a same magnitude for each of the voltage sources 102 to 112 to generate the voltages V_{COM} and V_1 to V_5. If any one of the gamma voltages V_{GCOM} and V_{G1} to V_{G5} is desired to be tuned individually, only the corresponding resistor among R_{COM} and R_1 to R_5 has to be changed. Furthermore, since the gamma voltages V_{G6} to V_{G10} are generated by mapping the gamma voltages V_{G5} to V_{G1}, respectively, with the common gamma voltage V_{GCOM} as the mapping reference, tuning the gamma voltages V_{COM} and V_1 to V_5 will automatically tuning the gamma voltages V_{G6} to V_{G10} in the same time.

A current mirror 30, as shown in Fig. 4, provides the gamma currents I_S for the resistors R_{COM} and R_1 to R_5, and the current mirror 30 comprises a reference branch 32 connected with a reference current I_{ref} provided by a current source 46, and several mirror branches 34, 36, 38, 40, 42 and 44 to mirror the reference current I_{ref}, respectively, to generate the respective gamma currents I_S for the resistors R_{COM} and R_1 to R_5 of the voltage sources 102 to 112. The current source 46 comprises a reference resistor R_S connected between ground GND and a transistor 462 that is further

connected to the reference branch 32, and an operational amplifier 464 with a non-inverted input connected to a reference voltage V_{ref}, an inverted input connected to the resistor RS and the transistor 462, and an output connected to the gate of transistor 462. For

$$I_S=I_{ref}=V_{ref}/R_S, \qquad \text{[EQ-1]}$$

adjustment of either the reference resistor R_S or the reference voltage V_{ref} will change the magnitude of the gamma current I_S.

Referring to Fig. 3 for the gamma voltage generator 100, the first group of the gamma voltages V_{G1} to V_{G5} and the other group of the gamma voltages V_{G6} to V_{G10} generated by mapping the first group of the gamma voltages V_{G1} to V_{G5} are symmetric to each other with respect to the common gamma voltage V_{GCOM} as the symmetric center, corresponding to a gamma curve 138 as shown in Fig. 5.

In more detail, using the symmetric property of the gamma curve, the common gamma voltage V_{GCOM} and the first gamma voltages V_{G1} to V_{G5} are generated first, and then the common gamma voltage V_{GCOM} is used as the center axis to map the first gamma voltages V_{G1} to V_{G5} to generate the second gamma voltages V_{G6} to V_{G10}. In other words, the first gamma voltages V_{G1} to V_{G5} and the second gamma voltages V_{G6} to V_{G10} are symmetric to each other with the common gamma voltage V_{GCOM} as their center. Since the second

gamma voltages V_{G6} to V_{G10} are directly generated from the common gamma voltage V_{GCOM} and the first gamma voltages V_{G1} to V_{G5}, no pins are required for them for the chip and thus the number of the pins are reduced by a half.

Fig. 6 shows an embodiment for the mirror mapping circuit 136 shown in Fig. 3. To generate the gamma voltage V_{G6}, for example, an operational amplifier 140 has a non-inverted input connected with the common gamma voltage V_{GCOM}, an inverted input connected with the gamma voltage V_{G5} through a resistor 142, and another resistor 144 connected between the inverted input and the output of the operational amplifier 140. For

$$(V_{G6} - V_{GCOM})/R_{144} = (V_{GCOM} - V_{G5})/R_{142}, \qquad \text{[EQ-2]}$$

where R_{144} and R_{142} are the resistances of the resistors 144 and 142, respectively, and when $R_{144} = R_{142}$, it is obtained

$$| V_{G6} - V_{GCOM} | = | V_{G5} - V_{GCOM} | , \qquad \text{[EQ-3]}$$

and obviously, the gamma voltages V_{G5} and V_{G6} are symmetric to each other with respect to V_{GCOM} as the center axis.

Fig. 7 shows another embodiment for the mirror mapping circuit 136 shown in Fig. 3. Again, to generate the gamma voltage

V_{G6}, three current mirrors 146, 148 and 150, and three resistors 152, 154 and 156 of a same resistance are used. The current mirror 146 has its reference branch 1462 connected to a current source 164, and its mirror branch 1464 connected to the resistor 154 and the mirror branch 1504 of the current mirror 150. The current source 164 provides a current I_1 for the reference branch 1462 according to the gamma voltage V_{GCOM}, and it comprises a resistor 152 connected between ground GND and a transistor 159 that is further connected to the reference branch 1462 of the current mirror 146, and an operational amplifier 158 with its non-inverted input connected to the gamma voltage V_{GCOM}, inverted input connected to the resistor 152, and output connected to the gate of the transistor 159. The current mirror 148 has a reference branch 1482 connected to a current source 166, and a mirror branch 1484 connected to the reference branch 1502 of the current mirror 150. The current source 166 provides a current I_3 for the reference branch 1482 according to the gamma voltage V_{G5}, and it comprises a resistor 156 connected between ground GND and a transistor 161 that is further connected to the reference branch 1482 of the current mirror 148, and an operational amplifier 160 with its non-inverted input connected to the gamma voltage V_{G5}, an inverted input connected to the resistor 156, and output connected to the gate of the transistor 161. M, N and P denoted in the three current mirrors 146, 148 and 150 represent the channel widths of the transistors besides thereto. Due to the gamma voltage V_{GCOM} connected to non-inverted input of

the operational amplifier 158, a voltage V_{GCOM}' is present on the inverted input of the operational amplifier 158 and applied to the resistor 152, and thus a current I_1 is induced on the reference branch 1462 of the current mirror 146. For the ratio of the channel widths of the transistors in the current mirror 146 is M:2M, the output of the mirror branch 1464 is double, i.e., $I_2 = 2 \times I_1$. On the other hand, due to the gamma voltage V_{G5} connected to the non-inverted input of the operational amplifier 160, a voltage V_{G5}' is present on the inverted input of the operational amplifier 160 and applied to the resistor 156, and thus a current I_3 is generated on the reference branch 1482 of the current mirror 148. For the ratio of the channel widths of the transistors in the current mirror 148 is N:N, the output of the mirror branch 1484 is the same, i.e., $I_4 = I_3$. The reference branch 1502 of the current mirror 150 receives the mirrored current I_4, and the ratio of the channel widths of the transistors in the current mirror 150 is P:P, it is thus obtained that the mirrored current $I_5 = I_4$, and further $I_5 = I_3$, since $I_4 = I_3$. The gamma voltage output from the node 162 is

$$V_{G6} = (I_2 - I_5) \times R_{154} = I_2 \times R_{154} - I_5 \times R_{154}, \qquad \text{[EQ-4]}$$

where R_{154} is the resistance of the resistor 154. Since the resistors 152, 154 and 156 have the same resistance, and $I_2 = 2 \times I_1$, $I_5 = I_3$, the gamma voltage

$$V_{G6} = (2\times I_1)\times R_{152} - (I_3)\times R_{156}$$
$$= 2(I_1\times R_{152}) - (I_3\times R_{156})$$
$$= 2V_{GCOM}' - V_{G5}' \qquad \text{[EQ-5]}$$

Based on the principle of the virtual short between the non-inverted and inverted inputs of an operational amplifier, the non-inverted and inverted inputs of the operational amplifiers 158 and 160 are the same voltages, that is

$$V_{GCOM} = V_{GCOM}',$$

and

$$V_{G5} = V_{G5}'.$$

As a result, from equation EQ-5,

$$V_{G6} = 2V_{GCOM}' - V_{G5}' = 2V_{GCOM} - V_{G5},$$

$$V_{G6} - V_{GCOM} = V_{GCOM} - V_{G5},$$

and

$$|V_{G6} - V_{GCOM}| = |V_{G5} - V_{GCOM}|. \qquad \text{[EQ-6]}$$

As for the situation of equation EQ-3, the gamma voltages V_{G5} and V_{G6} are symmetric to each other with respect to V_{GCOM} as the center axis.

While the present invention has been described in conjunction with preferred embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, it is intended to embrace all such alternatives, modifications and variations that fall within the spirit and scope thereof as set forth in the appended claims.